CBCS SCHEME

USN | | | | | | | | | | |

BIS714C

Seventh Semester B.E./B.Tech. Degree Examination, Dec.2025/Jan.2026
Embedded Systems

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Describe the elements of an embedded system with a block diagram.	8	L2	CO1
	b.	Give comparison between RISC and CISC architecture.	6	L2	CO1
	c.	i) Explain SRAM cel ii) Explain Big Endian and Little Endian operation and give examples.	6	L2	CO1
		OR			
Q.2	a.	Give the differences between a micro controller and micro processor.	8	L2	CO1
	b.	With neat diagram, explain the differences between Harvard and Von-Neumann architecture.	8	L2	CO1
	c.	Describe the functions of optocoupler I2C and IrDA for embedded system.	4	L2	CO1
		Module – 2			
Q.3	a.	Define and explain operational and non-operational quality attributes of an embedded system.	10	L2	CO2
	b.	With a functional block diagram, explain the working of a washing machine.	10	L2	CO2
		OR			
Q.4	a.	With a neat flow diagram, explain high level language sources file to machine language conversion.	6	L2	CO2
	b.	Compare Data Flow Graph (DFG) and Conditional Data Flow Graph (CDFG) model with an example.	6	L2	CO2
	c.	With the help of FSM model, explain the design and operation of automatic seat belt warning system.	8	L2	CO2
		Module – 3			
Q.5	a.	Define the term operating system with a neat diagram, explain the operating system architecture.	8	L2	CO2
	b.	Explain monolithic and micro Kernels with suitable examples for each.	6	L2	CO3
	c.	Explain task, process and threads.	6	L2	CO3

		OR			
Q.6	**a.**	Explain the concept of 'deadlock with a neat diagram. Mention the different conditions which favors a deadlock situation.	**10**	**L2**	**CO3**
	b.	With a block diagram, explain the embedded system development environment with function of the components used in brief.	**10**	**L2**	**CO3**
		Module – 4			
Q.7	**a.**	With a neat and labeled diagram, explain the ARM core dataflow model. Describe the function of major components such as the register file, ALU, barrel shifter and multiplier.	**10**	**L2**	**CO4**
	b.	With a neat and labelled diagram, explain register organization in the ARM processor. Also, describe the structure and function of the Current Program Status Register (CPSR).	**10**	**L2**	**CO4**
		OR			
Q.8	**a.**	Describe the different stages of the ARM pipeline [e.g, 3-stage for ARM7, 5-stage for ARM9 and 6-stage for ARM10] and what operation is performed in each stage.	**10**	**L2**	**CO4**
	b.	Describe the working of a simplified Von Neumann architecture with cache and a simplified Harvard architecture with TIMs.	**10**	**L2**	**CO4**
		Module – 5			
Q.9	**a.**	With a neat and labeled diagram, describe the data flow between the barrel shifter and the Arithmetic Logic Unit (ALU) in ARM data processing instructions. Explain the function of different shift operations – LSL, LSR, ASR, RDR and RRX.	**10**	**L2**	**CO5**
	b.	Explain in detail Arithmetic, Logical and comparison instruction in ARM.	**10**	**L3**	**CO5**
		OR			
Q.10	**a.**	Describe how LDR/STR and LDM/STM instruct operate, along with examples showing pre-indexing, post–indexing and auto increment/decrement addressing model.	**10**	**L3**	**CO5**
	b.	Explain the following ARM processor instructions : i) Software Interrupt (SWI) Instruction. ii) Program Status Register (PSR) Instruction	**10**	**L2**	**CO5**

* * * * *